NANO-ENABLED MEMORY DEVICES AND ANISOTROPIC CHARGE CARRYING ARRAYS

ABSTRACT OF THE DISCLOSURE

Methods and apparatuses for nanoenabled memory devices and anisotropic charge carrying arrays are described. In an aspect, a memory device includes a substrate, a source region of the substrate, and a drain region of the substrate. A thin film of nanoelements is formed on the substrate above a channel region. A gate contact is formed on the thin film of nanoelements. The nanoelements allow for reduced lateral charge transfer. The memory device may be a single or multistate memory device. In a multistate memory device, nanoelements are present having a plurality of charge injection voltages, to provide multiple states. In another aspect, a printing device includes a charge diffusion layer that includes a matrix containing a plurality of nanoelements configured to be anisotropically electrically conductive through the charge diffusion layer to transfer charge to areas of the first surface with reduced lateral charge spread.

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